

REMARKS/ARGUMENTS

The timely filed Reply is in response to the Office Action dated June 29, 2004. In the Office Action, six claims (1-6) were pending, and all claims were rejected. In this Reply, claim 1 has been amended and claim 16 and 17 have been added. No new matter has been added.

Claims 1-6 were rejected under 35 U.S.C. §103(a) based on a paper entitled "High quality GaN grown on Si(111) by gas source molecular beam epitaxy with ammonia" by Nikishin et al in ("Nikishin") in view of U.S. Patent No. 5,563,428 to Ek et al ("Eck").

According to the Examiner:

Regarding claim 1, Nikishin et al. discloses an article comprising (see pages 2073-2074 and Fig. 1):

a crystal silicon substrate Si(111);
a buffer layer AlN disposed on substrate;
a single crystal group III-nitride layer (GaN) disposed on the layer AlN. Nikishin et al. discloses the layer disclosed on the substrate is made of AlN but fails to disclose the layer is made of silicon oxynitride. Ek et al. discloses the article comprising the Si substrate 1 and the silicon oxynitride layer 2 disposed on the substrate (lines 2-3, Col. 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use silicon oxynitride layer instead of AlN as disclosed in Ek et al. because silicon oxynitride layer formed on the crystal silicon substrate would reduce the difference in lattice parameters, reduce the strength of the Si-N bond between silicon of SiNO layer and nitrogen of GaN layer, improve thermal stability, low stress, and crack resistance in order to enhance a high quality GaN.

Before reviewing the cited art, Applicants will first review the claimed invention as recited in claim 1. Claim 1 recites a layered article, comprising a single crystal silicon comprising substrate, a silicon oxynitride layer (Si_xNyO_z) disposed on said silicon substrate, and a *single crystal* group III-nitride (e.g. GaN) layer disposed on and in contact with the silicon oxynitride layer.

In a preferred embodiment, the thickness of the silicon oxynitride layer (Si_xNyO_z) is less than 100 angstroms (new claim 16), in a more preferred embodiment 15 to 50 angstroms (claim

17), and in an even more preferred embodiment 15 to 40 angstroms (claim 4). The use of a thin silicon oxynitride layer provides a new and unexpected result which is different in kind and not merely degree from results of the prior art. Specifically, the thin (SixNyOz) layer of less than 100 angstroms was unexpectedly found to permit high quality single crystal Group III-N layers (e.g. GaN) to be deposited thereon, as evidenced by, for example, by the XRDs shown in Figs. 6 and 7, and the PL spectra shown in Fig. 9. Prior to Applicants invention articles having GaN directly on SixNyOz was unknown as evidenced by the need for intermediate "buffer" layers (e.g. AlN in Nikishin and Ek, as well as GaAs, AlAs, SiC, SiO_2 , Si_3N_4 and ZnO) to permit formation of substantially single crystal GaN when using a Si or other substrate.

Applicants agree with the Examiner's characterization of Nikishin, that being GaN/AlN buffer layer/Si substrate, but fails to disclose the buffer layer is made of silicon oxynitride. In addition, Applicants also agree that in one embodiment Ek discloses a silicon oxynitride layer on Si. However, as described below, Applicants respectfully disagree with the Examiner's assertion that "It would have been obvious to one having ordinary skill in the art at the time the invention was made to use silicon oxynitride layer instead of AlN as disclosed in Ek".

Ek discloses a structure comprising a substrate, a dielectric layer formed over the substrate, and a single crystal layer of a compound formed over the dielectric layer. The single crystal layer is formed by the chemical reaction of at least a first element with an initial single crystal layer of a second element on the dielectric layer having an initial thickness of about 100 to about 10,000 angstroms. According to another aspect, a carbide single crystal layer is provided on a substrate by depositing carbon from a solid carbon source at a low rate and low temperature, followed by reacting the carbon with the underlying layer to convert it to the carbide.

Referring to Fig. 1, the following is noted beginning on col. 2. lines 66 to col. 3 line 43:

FIG. 1 is a schematic representation of forming a structure of the present invention. In particular, a substrate 1, such as silicon, is provided, over which is provided a dielectric layer 2. Examples of suitable dielectric layer 2 are glasses such as silicon dioxide, silicon oxynitrides and borosilicates. The dielectric layer is typically about 1000 to about 20,000 angstroms thick, preferably about 1,000 to about 5,000 angstroms thick, and most preferably about 2,000 angstroms thick.

The dielectric layer can be provided by any known technique, such as CVD (chemical vapor deposition) and in the case of silicon oxide or silicon dioxide by thermal oxidation of the silicon substrate.

A relatively thin layer 3 of a crystalline material is formed over the dielectric layer 2. This layer 3 has a thickness of about 100 to about 10,000 angstroms, preferably about 200 to about 1,000 angstroms, and most preferably about 200 to about 300 angstroms. It is critical to the success of this invention that the layer 3 be relatively thin and be crystalline. The layer is preferably silicon. This layer 3 can be formed by any conventional technique, such as by the bond and etch back technique (BESOI) or by Simox, or by lateral epitaxial overgrowth.

This layer 3 is then converted to a single crystal layer of a compound by chemical reaction with a second and different element.

FIG. 1 illustrates depositing as the second element 4 carbon. Other elements are germanium, cobalt, titanium and tantalum. The carbon can be deposited from a solid carbon source or less preferably by heterogeneous gas phase nucleation.

The thickness of layer 4 is kept equal or at least substantially equal .+- .10% to the layer 3 thickness, which is thin enough to form a homogeneous single crystal layer without the nucleation of defects.

The layer 3/layer 4 bilayer (e.g. C/Si) is then reacted at temperatures typically about 900-1,770 K, and preferably 1,070-1,170 K to form a uniform single crystal layer 5. The rate of reaction is directly related to the temperature and it is preferred to maintain the temperature as low as possible (e.g. --1,070 K) for control of the quality of layer 5. In the case of silicon and carbon, such layer is silicon carbide, which is usually 3c-SiC. This layer 5 can then be used as a template for further deposition of silicon carbide or some other semiconductor.

In Fig. 3 which is Ek's most relevant embodiment to Applicants' claimed invention, Ek discloses a blue LED structure which includes GaN (5)/AlN(4)/SiC(3)/silicon dioxide(2)/Si (1). Thus, although Ek discloses a silicon oxynitride layer (2) (see Fig. 1 and 2), this layer is disposed

on top of a Si substrate, then a thin crystalline Si film is grown on top of oxynitride or other dielectric material, such as silicon dioxide. SiC(3) could be formed by reaction with carbon containing species (See Fig. 1) or by reacting silicon with acetylene (C_2H_2) (see Fig. 2).

Ek clearly teaches away from forming GaN directly on silicon oxynitride for at least the following reason. If the Examiner's assertion above that it "would have been obvious to one having ordinary skill in the art at the time the invention was made to use silicon oxynitride layer instead of AlN as disclosed in Ek et al. because silicon oxynitride layer formed on the crystal silicon substrate would reduce the difference in lattice parameters, reduce the strength of the Si-N bond between silicon of Si₃N₄ layer and nitrogen of GaN layer, improve thermal stability, low stress, and crack resistance in order to enhance a high quality GaN" were true, Ek would not have used AlN (4) as a buffer layer for GaN (5). (see Figs. 3 and 4). Such additional processing adds numerous process steps and expense process to first form a SiC layer (3), then AlN buffer layer (4) and finally the GaN layer (5). Had the Examiner's assertion been true, Ek would have instead deposited the GaN as layer (3) directly on the silicon oxynitride (2) on Si (1) (Applicants' claimed invention). Thus, Ek clearly teaches away from forming GaN directly on silicon oxynitride.

As noted above, Nikishin discloses GaN/AlN buffer layer/Si substrate. Ek teaches GaN/AlN/SiC, the SiC being formed using thin crystalline Si film and carbon compounds on a dielectric (including silicon oxynitride) on Si). Therefore, Ek strongly teaches away from deposition of GaN directly on silicon oxynitride. Accordingly, Applicants submit that amended claim 1 and all claims dependent thereon are patentable claims.

Some claims include independently patentable limitations. For example, claims which recite the thickness of Applicants' claimed silicon oxynitride layer, such as 100 angstroms (new

claim 16), 15 to 50 angstroms (new claim 17), and 15 to 40 angstroms (claim 4) recite independently patentable limitations. As noted above, Ek discloses a silicon oxynitride thickness of "typically about 1000 to about 20,000 angstroms thick, preferably about 1,000 to about 5,000 angstroms thick, and most preferably about 2,000 angstroms thick."

As noted above, thin (SixNyOz) of 100 angstroms or less directly below a single crystal III-N compound semiconductor (e.g. GaN) is not obtainable through routine experimentation and "provides a new and unexpected result which is different in kind and not merely degree from results of the prior art." Specifically, as noted above, the thin (SixNyOz) of less than 100 angstroms was unexpectedly found to produce high quality single crystal GaN layers. Accordingly, Applicants submit that claims 4, 16 and 17 recite independently patentable limitations.

Applicants have made every effort to present claims which distinguish over the cited art; and it is believed that all claims are now in condition for allowance. However, the Examiner is invited to call the undersigned (at 561-671-3662) if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. The Commissioner for Patents is hereby authorized to charge any deficiency in fees due with the filing of this document and during prosecution of this application to Deposit Account No. 50-0951.

Respectfully submitted,
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